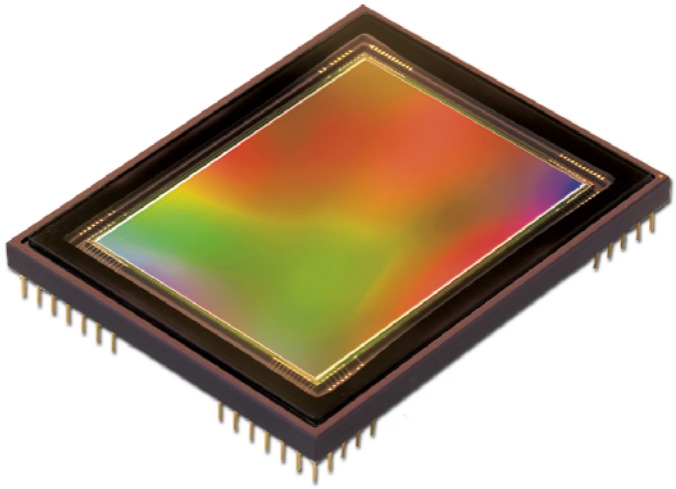
DATA SHEET



FTF4052C

22M Full-Frame CCD Image Sensor

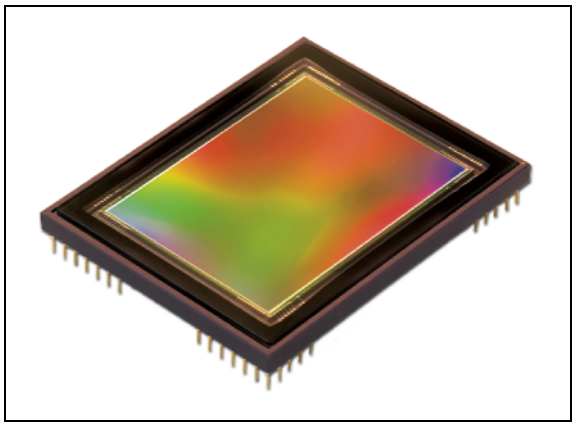
Product specification

2009 April 24

DALSA
Professional Imaging

22M Full-Frame CCD Image Sensor FTF4052C

- **Image format (36 x 48 mm^2)**
- **22M active pixels (4008H x 5344V)**
- **RGB Bayer pattern**
- **Progressive scan**
- **Excellent antiblooming**
- **Variable electronic shuttering**
- **Square pixel structure**
- **H and V binning**
- **Vertical subsampling**
- **80% optical fill factor**
- **High linear dynamic range (>72dB)**
- **High sensitivity**
- **Low dark current and fixed pattern noise**
- **Low readout noise**
- **Data rate up to 27 MHz**
- **Mirrored, split and four quadrant readout**
- **Perfectly matched to visual spectrum**
- **RoHS compliant**



Description

The FTF4052C is a full frame CCD colour image sensor designed for professional digital photography applications, with very low dark current and a linear dynamic range of over 12 true bits at room temperature. The four low-noise output amplifiers, one at each corner of the chip, make the FTF4052C suitable for a wide range of high-end visual light applications. With one output amplifier, a progressively scanned image can be read out at one frame per second. By using multiple outputs, the frame rate increases accordingly. The device structure is shown in figure 1.

Device structure

Optical size:	36.072 mm (H) x 48.096 mm (V)	
Chip size:	38.452 mm (H) x 49.796 mm (V)	
Pixel size:	9 µm x 9 µm	
Active pixels:	4008 (H) x 5344 (V)	
Total no. of pixels:	4056 (H) x 5356 (V)	
Optical black pixels:	Left: 20	Right: 20
Timing pixels:	Left: 4	Right: 4
Dummy register cells:	Left: 24	Right: 24
Optical black lines:	Bottom: 6	Top: 6

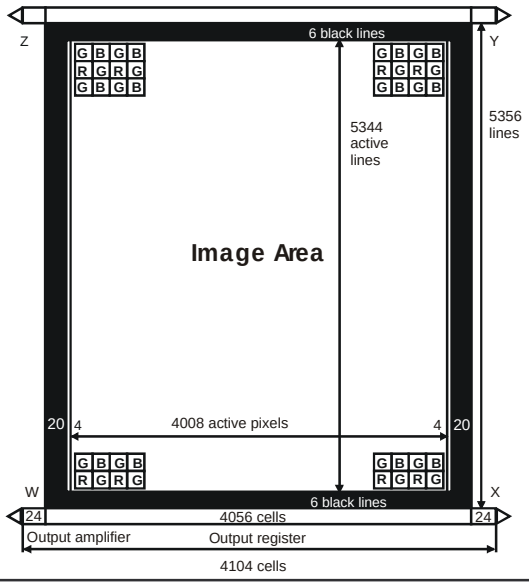


Figure 1 - Device structure

Architecture of the FTF4052C

The optical centres of all pixels in the image section form a square grid. The charge is generated and integrated in this section. Output registers are located below and above the image section for readout. After the integration time, the image charge is shifted one line at a time to either the upper or lower register or to both simultaneously, depending on the readout mode. A separate transfer gate (TG) between the image section and output register will enable sub-sampling features. The left and right half of each register can be controlled independently. This enables either single or multiple read-out. During vertical transport, the C3 gates separate the pixels in the register. The central C3 gates of the lower and upper registers are part of the left half of the sensor (W and Z quadrants respectively). Each register can be used for vertical binning. Each register contains a summing gate at both ends that can be used for horizontal binning (see figure 2).

IMAGE SECTION	
Image diagonal (active video only)	60.1 mm
Aspect ratio	3:4
Active image width x height	36.072 x 48.096 mm^2
Pixel width x height	9 x 9 μm^2
Geometric fill factor	80%
Image clock pins	16 pins (A1...A4)
Capacity of each clock phase	38nF per pin
Number of active lines	5344
Number of black reference lines	4 (=2x2)
Number of dummy black lines	8 (=2x4)
Total number of lines	5356
Number of active pixels per line	4008
Number of overscan (timing) pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)
Total number of pixels per line	4056

OUTPUT REGISTERS	
Output buffers on each corner	Three-stage source follower
Number of registers	2
Number of dummy cells per register	48 (2x24)
Number of register cells per register	4104 (4056 + 48)
Output register horizontal transport clock pins	6 pins per register (C1...C3)
Capacity of each C-clock phase	200 pF per pin
Overlap capacity between neighbouring C-clocks	40pF
Output register Summing Gates	4 pins (SG)
Capacity of each SG	15pF
Reset Gate clock phases	4 pins (RG)
Capacity of each RG	15pF

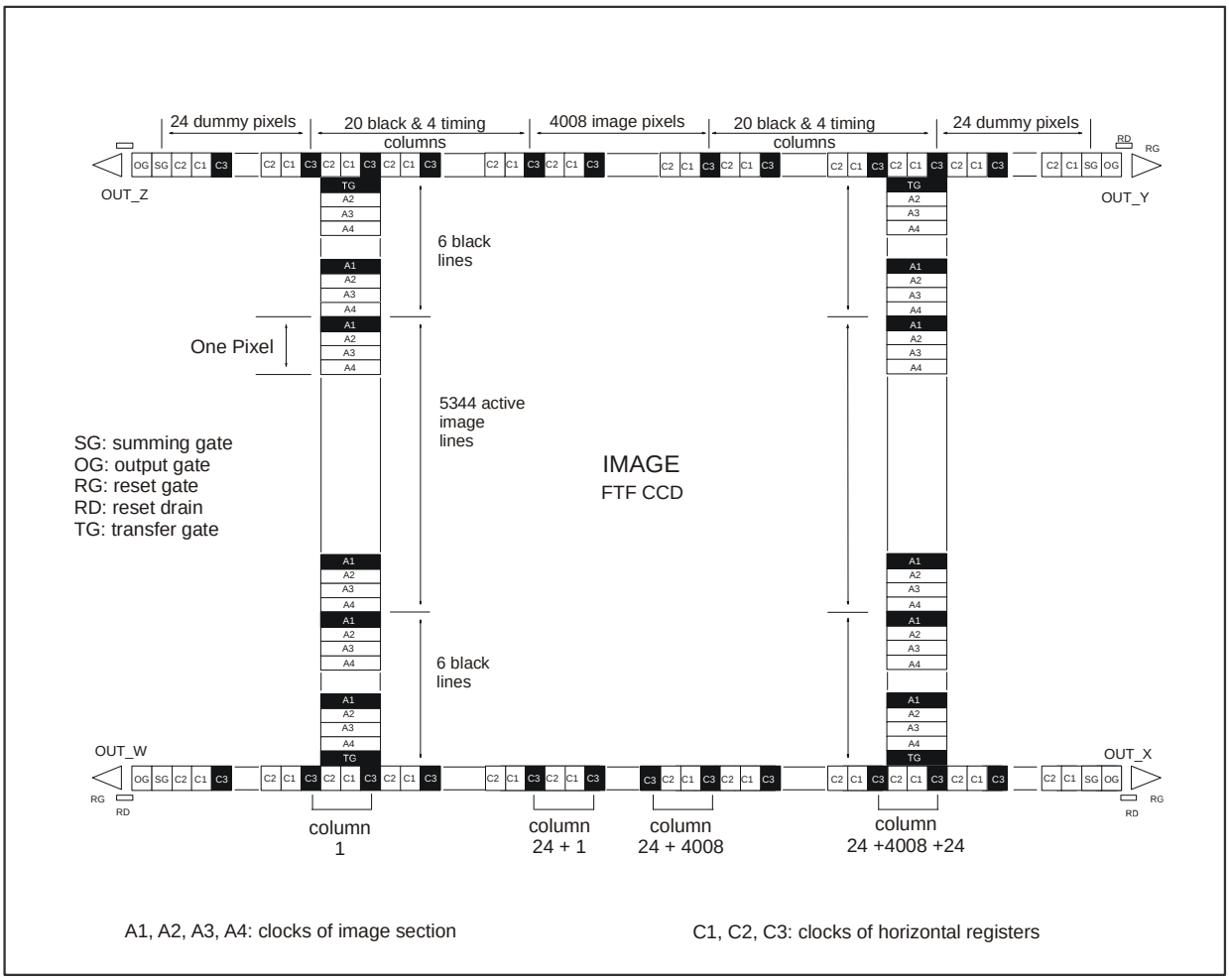


Figure 2 - Detailed internal structure

Specifications

ABSOLUTE MAXIMUM RATINGS[1]	MIN	MAX	UNIT
GENERAL:			
storage temperature	-40	+80	ºC
ambient temperature during operation	-20	+60	ºC
voltage between any two gates	-20	+20	V
DC current through any clock (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	+10	mA
VOLTAGES IN RELATION TO VPS:			
VPS, SFD, RD	-0.5	+30	V
VCS, SFS	-8	+5	V
All other pins	-5	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
VCS, SFS, VPS	-30	+0.5	V
All other pins	-30	+0.5	V
VOLTAGES IN RELATION TO SFD:			
RD	-5	0	V

DC CONDITIONS[2,3]		MIN [V]	TYPICAL [V]	MAX [V]	MAX [mA]
VNS[4]	N substrate	20	24	28	15
VPS	P substrate	5.5	6	6.5	15
SFD	Source Follower Drain	19.5	20	20.5	4.5
SFS	Source Follower Source	0	0	0	1
VCS	Current Source	0	0	0	–
OG	Output Gate	4.75	5.0	5.25	–
RD	Reset Drain	19.5	20	20.5	–

AC CLOCK LEVEL CONDITIONS[2]	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS/ TRANSFER GATES[5]:				
A-clock amplitude during integration and hold	8	8	8.5	V
A-clock amplitude during vertical transport (duty cycle=5/8) [6]	11	11	11.5	V
A-clock low level	-	0	-	V
Charge Reset (CR) level on A-clock[7]	-5	0	-	V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport=3/6)	4.75	5	5.25	V
C-clock low level	-	3	-	V
Summing Gate (SG) amplitude	4.75	5	10	V
Summing Gate (SG) low level	-	4.5	-	V
OTHER CLOCKS:				
Reset Gate (RG) amplitude	5	5	10	V
Reset Gate (RG) low level	-	17.0	-	V
Charge Reset (CR) pulse on Nsub[7]	0	5	5	V

[1] During Charge Reset it is allowed to exceed maximum rating levels (see note 7)
[2] All voltages in relation to SFS; typical values are according to test conditions
[3] Power-up sequence: VNS, SFD, RD, VPS, all others. The difference between SFD and RD should not exceed 5V during power up or down.
[4] To set the VNS voltage for optimal Vertical Antiblooming (VAB), it should be adjustable between minimum and maximum values
[5] Transfer gate should be clocked as A1 during normal transport or held low during a line shift to sub-sample image
[6] Three-level clock is preferred for maximum charge; the swing during vertical transport should be 3V higher than the voltage during integration
A two level clock (typically 10V) can be used if a lower maximum charge handling capacity is allowed
[7] Charge Reset can be achieved in two ways of which the first method is preferred:
A. The typical A-clock low level is applied to all image clocks for proper CR, an additional Charge Reset pulse on VNS is required
B. The minimum CR level is applied to all image clocks simultaneously

Timing diagrams (for default operation)

AC CHARACTERISTICS	MIN	TYPICAL	MAX	UNIT
Horizontal frequency (1/Tp)[1]	-	25	27	MHz
Vertical frequency	-	50	100	kHz
Charge Reset (CR) time	10	Line time	-	µs
Rise and fall times: image clocks (A)	10	20	-	ns
register clocks (C)[2]	3	5	1/8 Tp	ns
summing gate (SG)	3	5	1/8 Tp	ns
reset gate (RG)	-	3	1/8 Tp	ns

[1] TP = 1 clock period
[2] Duty cycle = 3/6

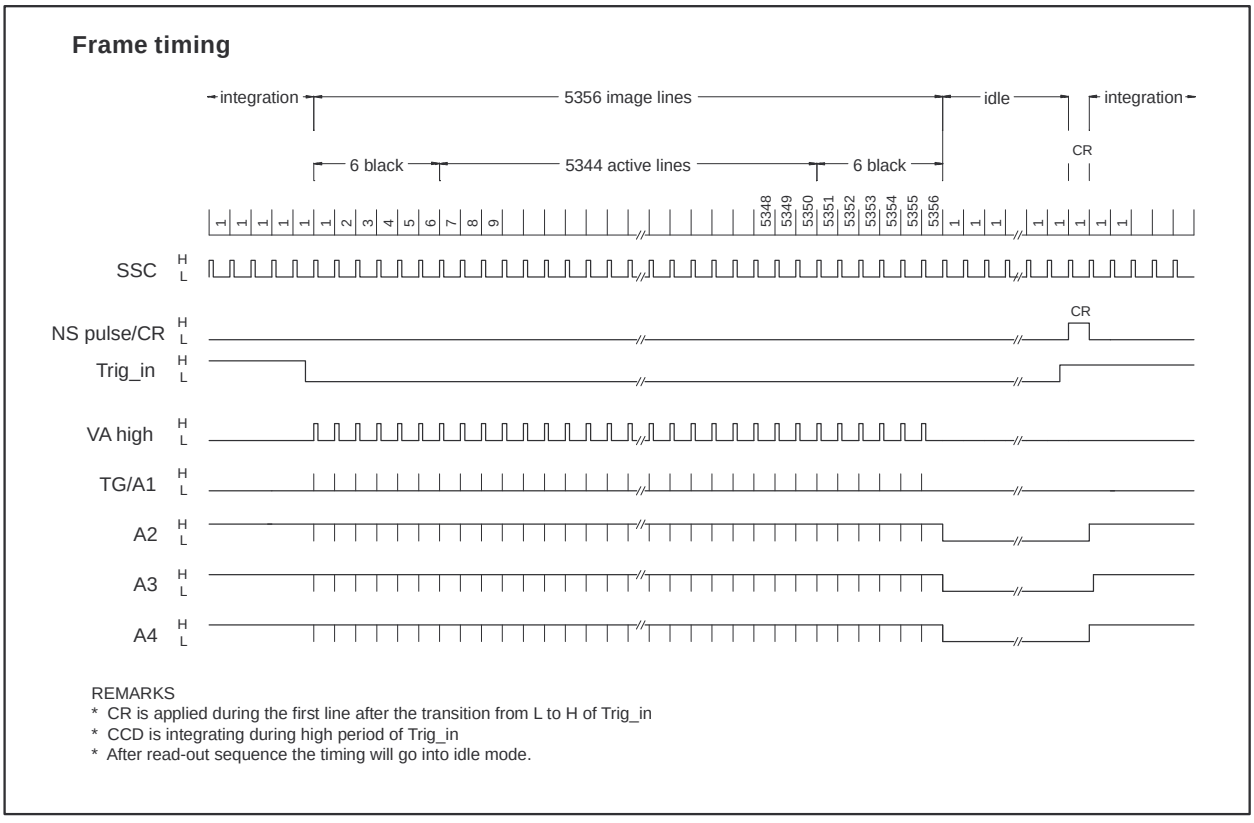
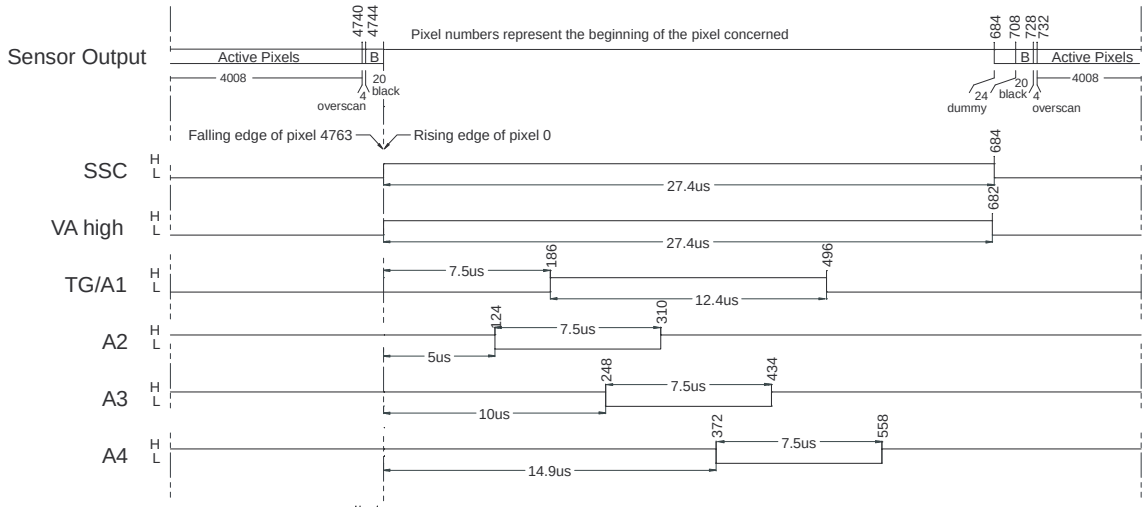


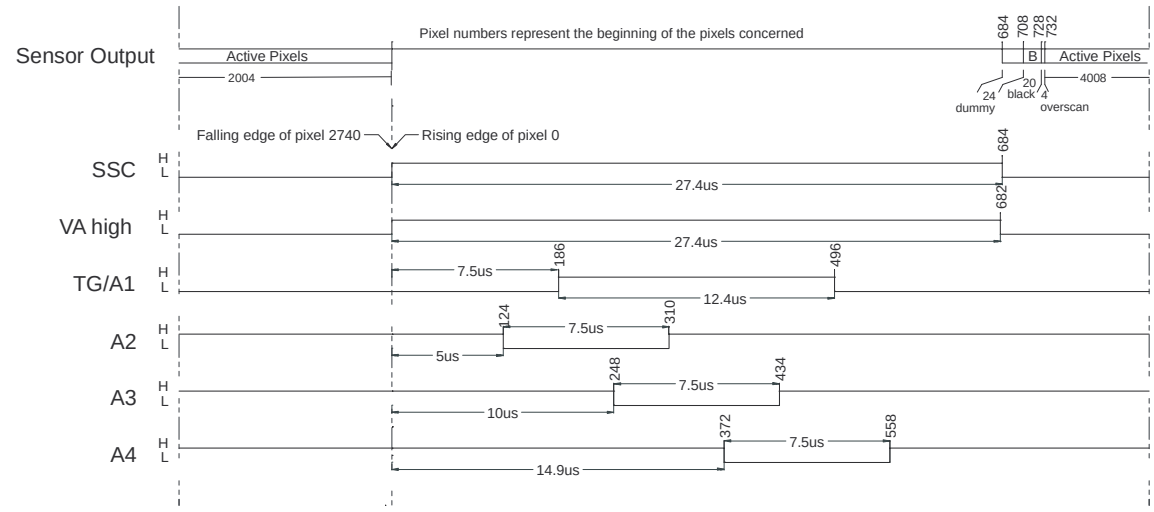
Figure 3 - Frame timing diagram

Line timing - single output



REMARKS
* Thorizontal = 4764 * 1/25E6 = 190.6us
* Vertical transport frequency = 50kHz

Line timing - dual output



REMARKS
* Thorizontal = 2740 * 1/25E6 = 109.6us
* Vertical transport frequency = 50kHz

Figure 4 - Vertical read-out, single and dual modes

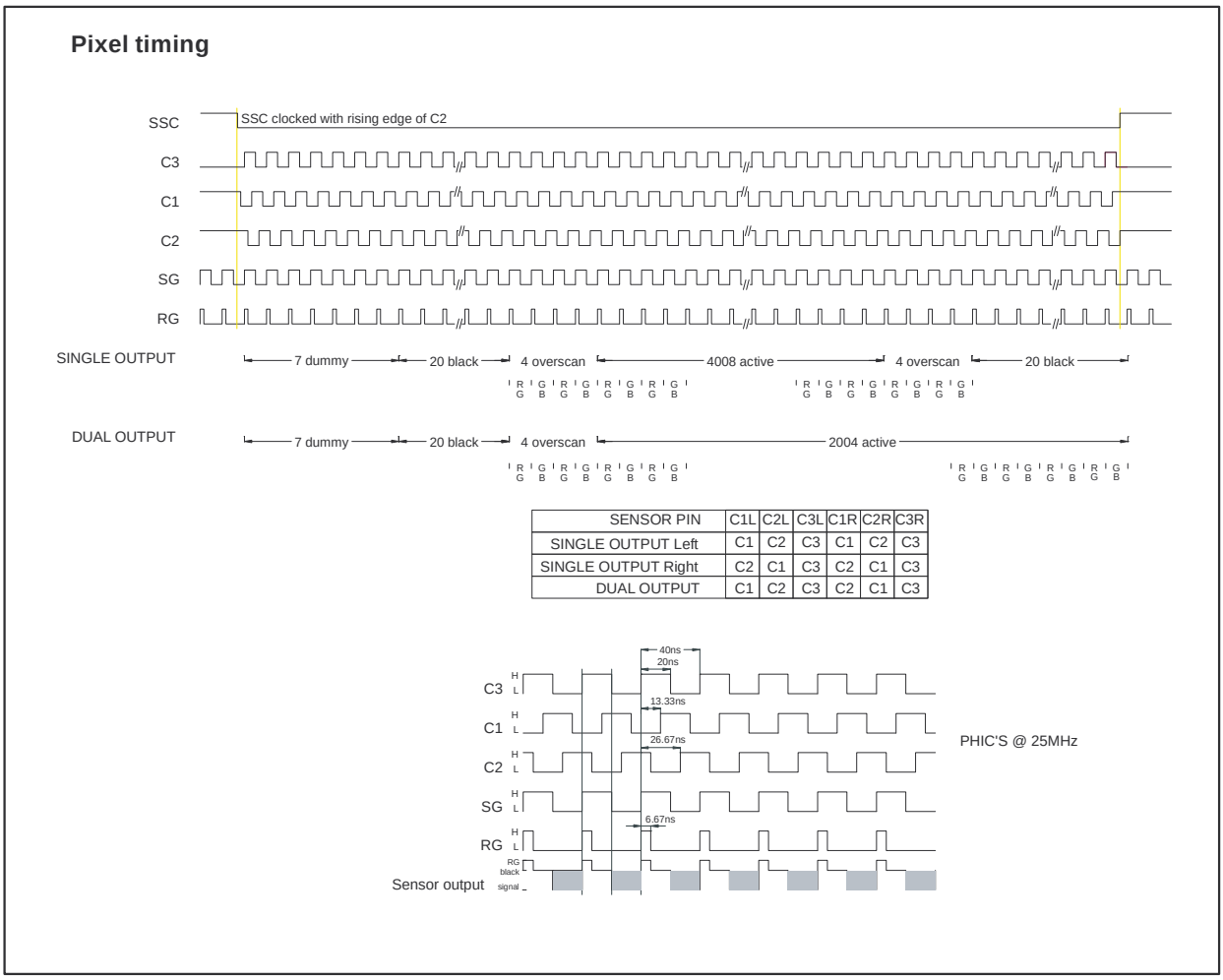


Figure 5 - Start horizontal read-out, single and dual modes

Performance

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper Vertical Antiblooming
- Sensor temperature=60°C (333K)
- Horizontal transport frequency=18MHz
- Vertical transport frequency=50kHz
- Integration time=100ms
- The light source is a lamp of 3200K in conjunction with neutral density filters and a 1.7mm thick BG40 infrared cut-off filter. For Linear Operation measurements, a temperature conversion filter (Melles Griot type no. 03FCG261, -120 mired, thickness: 2.5mm) is applied

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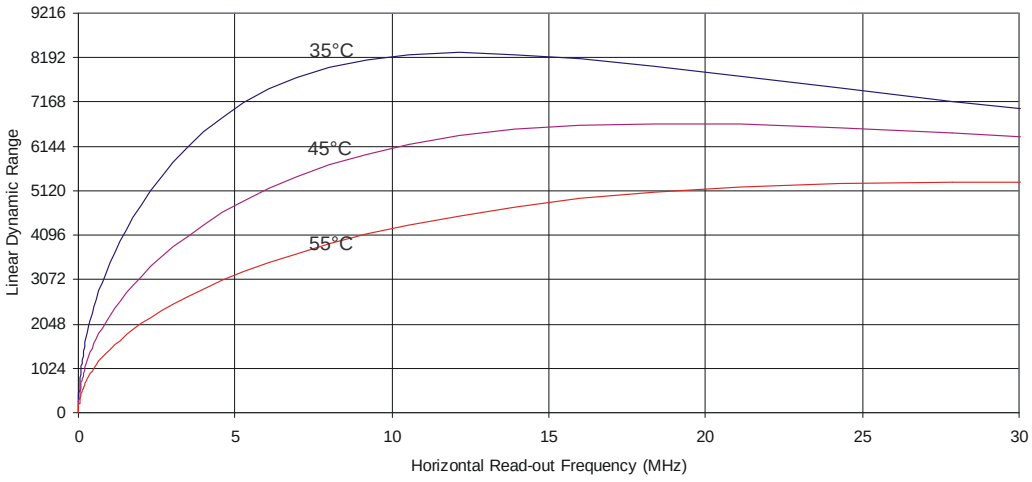
LINEAR OPERATION	MAX	TYPICAL	MAX	UNIT
Charge Transfer Efficiency[1]	-	0.999999	-	-
Image lag	-	0	0	%
Resolution (MTF) @56 lp/mm	65	-	-	%
Light sensitivity green pixels (530 nm)	700	1000	1300	mV/lux s
Red/Green ratio	65	80	95	%
Blue/Green ratio	45	60	75	%
Block-to-block difference	-	0.3	1.0	%
Stitching effect	-	0.7	3.0	%
Low Pass Shading[2]	-	2	5	%
Random Non-Uniformity (RNU)[3]	-	1	5	%

[1] Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer
[2] Low Pass Shading is defined as the ratio of the one-σ value of an 8x8 pixel blurred image (low-pass) to the mean signal value
[3] RNU is defined as the ratio of the one-σ value of the high-pass image to the mean signal of nominal light



Linear dynamic range is defined as the ratio of Q_{lin} to read-out noise with the read-out noise reduced by CDS.

Figure 6 - Typical Linear dynamic range vs. horizontal read-out frequency and sensor temperature

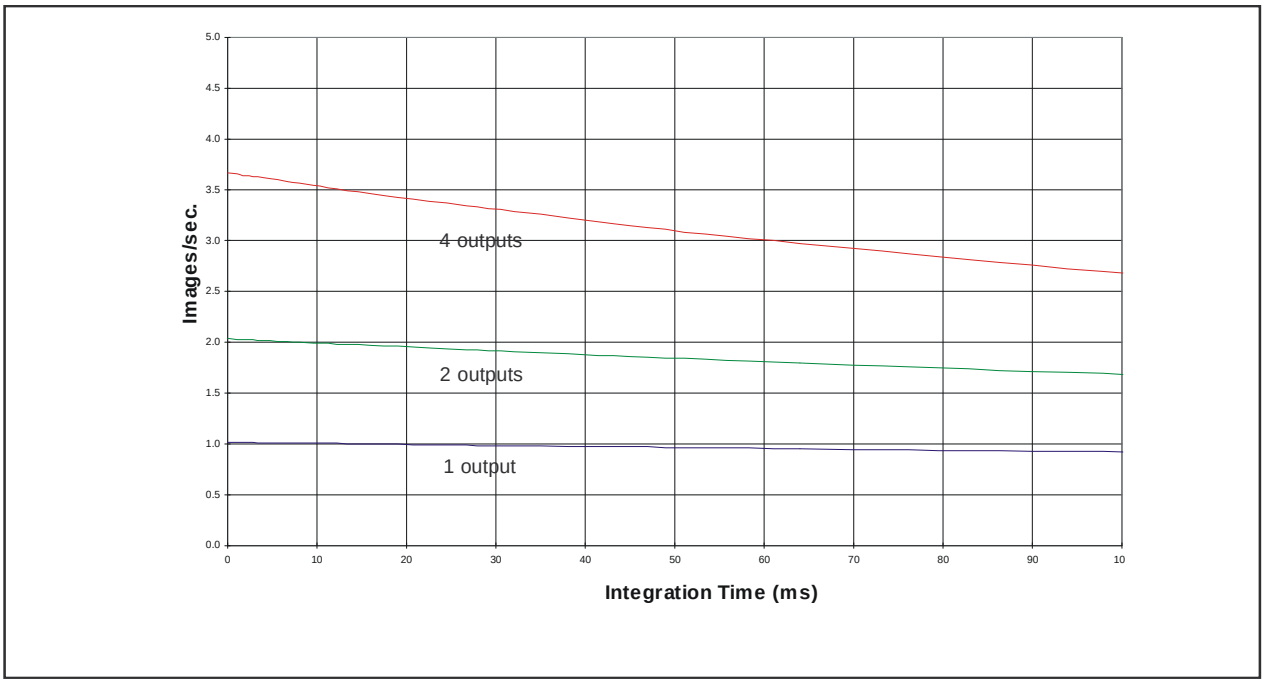


Figure 7 - Maximum number of images/second versus integration time

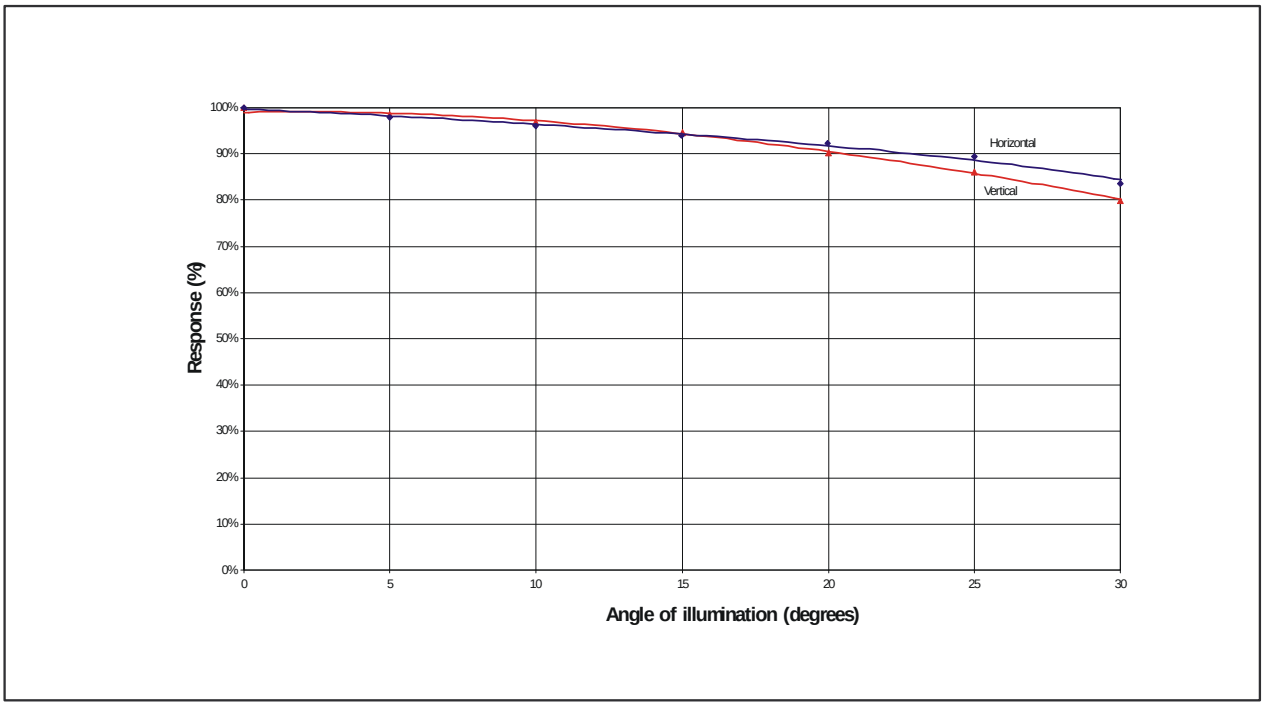


Figure 8 - Angular response versus angle of illumination

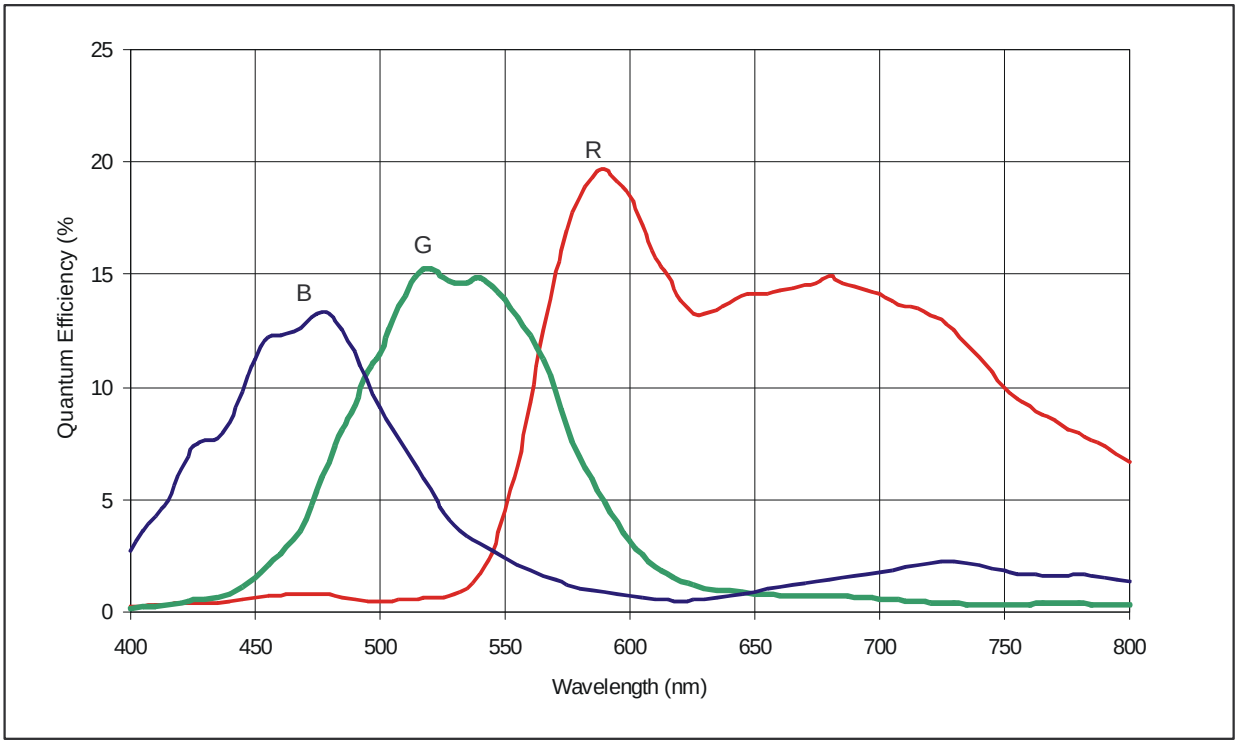


Figure 9 - Quantum efficiency versus wavelength

LINEAR/SATURATION	MIN	TYPICAL	MAX	UNIT
Full-well capacity saturation level (Qmax)[1]	2000	3400	-	mV
Full-well capacity linear operation (Qlin)[2]	2000	2500	-	mV
Charge handling capacity[3]	-	6000	-	mV
Overexposure[4] handling	-	200	-	x Qmax level

[1]Qmax is determined from the low-pass filtered image
[2]The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The test guarantees 97% linearity.
[3]Charge handling capacity is the largest charge packet that can be transported through the register and read out through the output buffer.
[4]Overexposure over entire area while maintaining good Vertical Anti-blooming (VAB) is tested by measuring the dark line along the image section.

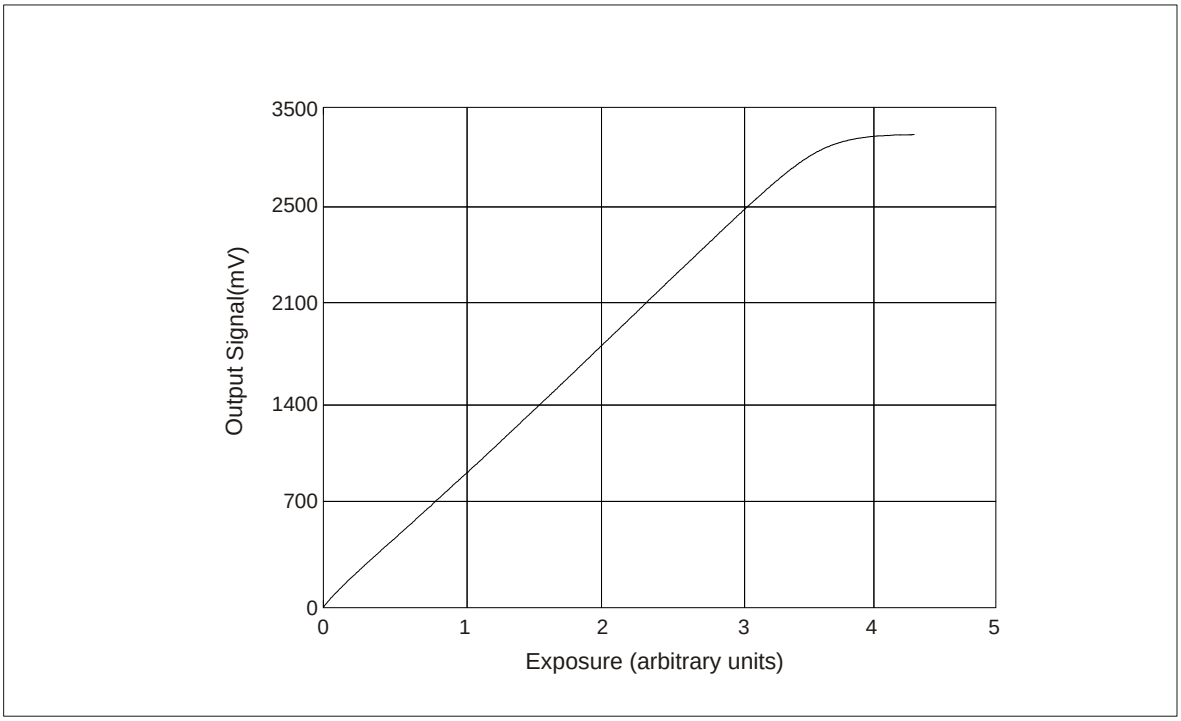


Figure 10 - Charge handling

OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Conversion factor	18	20	22	µV/el.
Mutual conversion factor matching (ΔACF)[1]	-	0	2	µV/el.
Supply current	-	4.5	-	mA
Bandwidth (R_{load}=3.3Ω)	90	105	-	MHz
Output impedance buffer (R_{load}=3.3kΩ, C_{load}=2pF	-	400	-	Ω

[1]Matching of the four outputs is specified as ΔACF with respect to reference measured at the operating point (Q_{lin}/2)

DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current level @ 20°C	-	10	30	pA/cm^2
Dark current level @ 60°C	-	0.3	0.6	nA/cm^2
Fixed Pattern Noise[1] (FPN) @ 60ºC	-	40	60	mV/s
Amplifier noise over full bandwidth after CDS	-	0.5	-	mV

[1]FPN is one-σ value of the high-pass image and normalized at 1 sec integration time

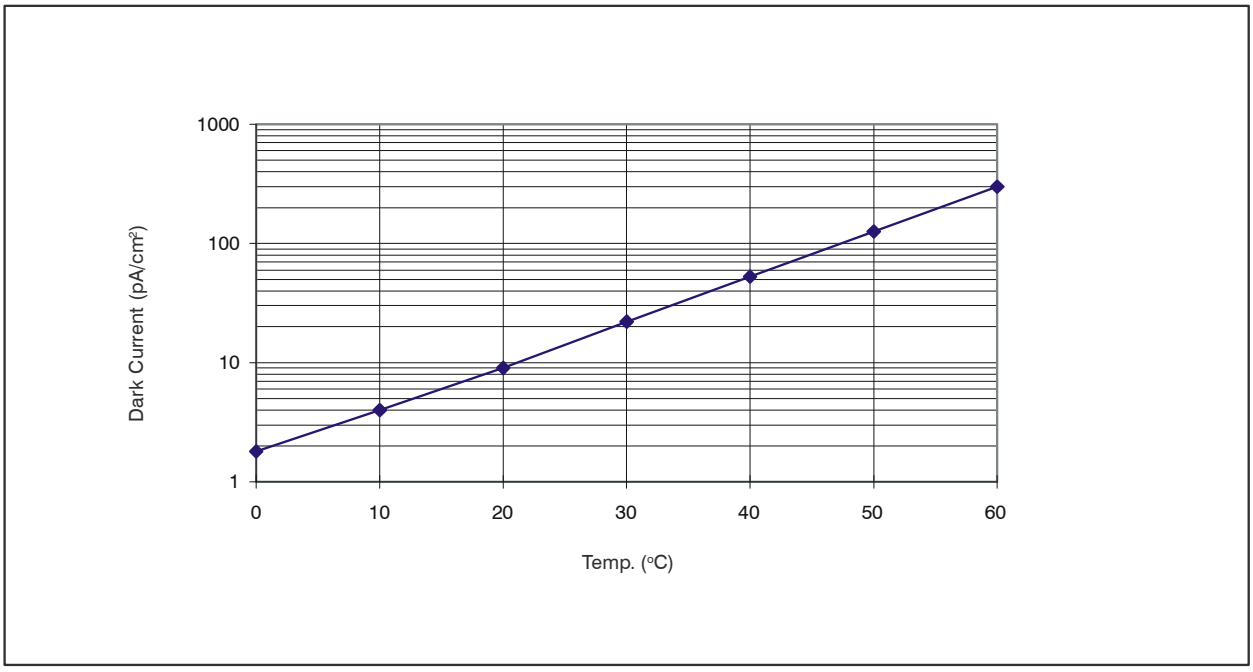


Figure 11 - Dark current versus temperature

Application information

Current handling
One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure, a total current of 5 to 10mA through all VPS connections together may be expected. The PNP emitter follower in the circuit diagram (figure 12) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure, a total current of 5 to 10mA through all VNS connections together may be expected. The clamp circuit, consisting of the diode and electrolytic capacitor, enable the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages
All DC voltages (not VNS, which has additional CR pulses as described above) should be uncoupled with a 22nF uncoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current,which will float through VRD. Therefore, a large series resistor in the VRD connection may be used.

Outputs
To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3Ω typically results in a bandwidth of 85MHz.

Device protection
The output buffers of the FTF4052C are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 12.

Unused sections
To reduce power consumption, the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

Device Handling

An image sensor is an MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remains undamaged. When handling the sensor, use fingercots.

When cleaning the glass, we recommend using ethanol (or possible water). Use of other liquids is strongly discouraged:

- if the the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches which can destroy the device.

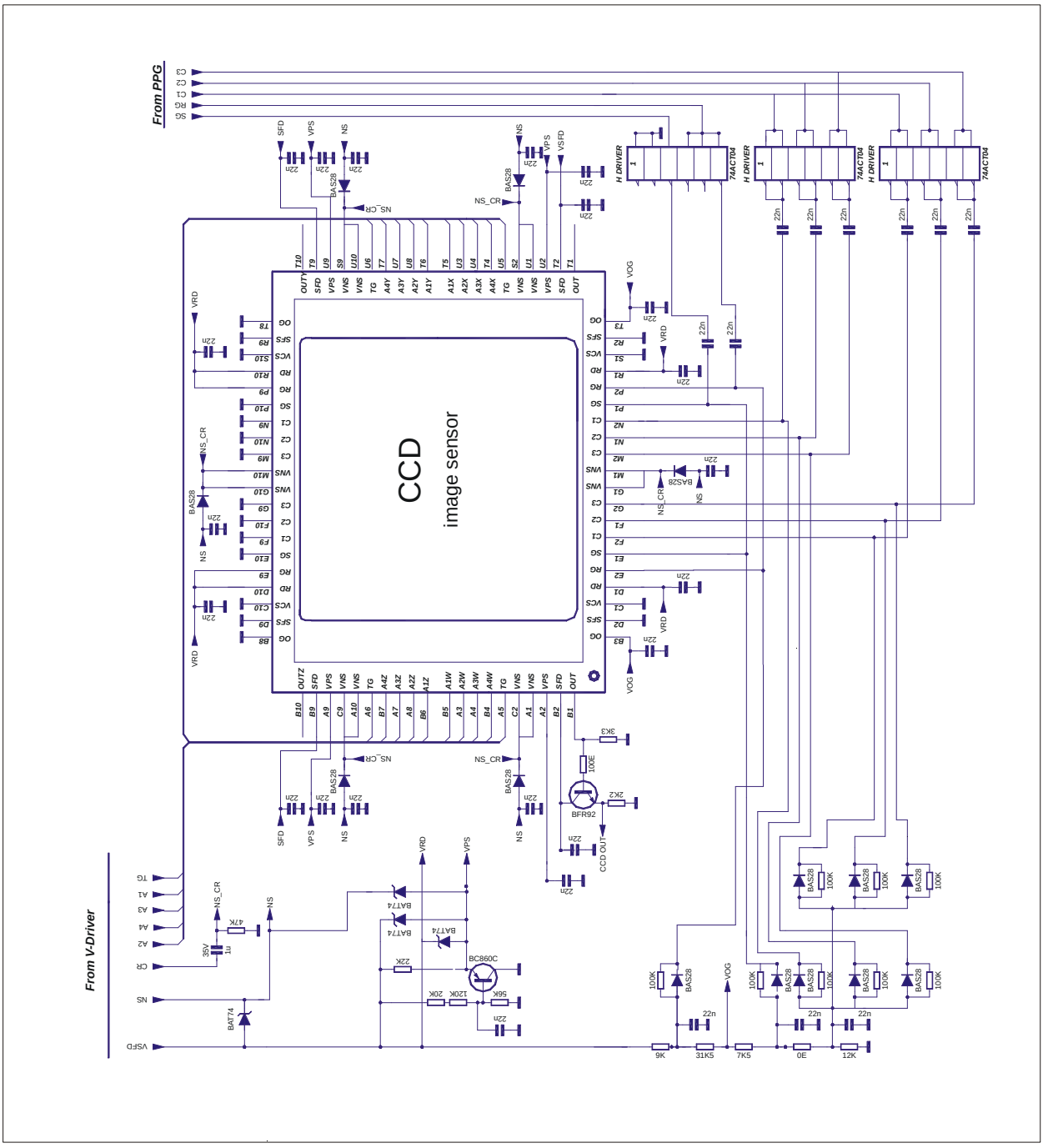


Figure 12 – Application diagram for single output operation

Pin configuration

The FTF4052C is mounted in a Pin Grid Array (PGA) package with 80 pins in a 20x25 grid of 51.30 x 64.00mm^2. The position of pin A1 (quandrant W) is marked with a gold dot on top of the package. The image clock phases of quadrant W are internally connected to X, and Y is connected to Z.

SYMBOL	LINEAR/SATURATION	PIN # W	PIN # X	PIN # Y	PIN # Z
VNS	N substrate	A1	P1	P10	A10
TG	N substrate	A5	P5	P6	A6
VNS	N substrate	C2	M2	M9	C9
VNS	N substrate	G1	H1	H10	G10
VPS	P substrate	A2	P2	P9	A9
SFD	Source Follower Drain	B2	N2	N9	B9
SFS	Source Follower Source	D2	L2	L9	D9
VCS	Current Source	C1	M1	M10	C10
OG	Output Gate	B3	N3	N8	B8
RD	Reset Drain	D1	L1	L10	D10
A1	Image Clock (Phase 1)	B5	N5	N6	B6
A2	Image Clock (Phase 2)	A3	P3	P8	A8
A3	Image Clock (Phase 3)	A4	P4	P7	A7
A4	Image Clock (Phase 4)	B4	N4	N7	B7
C1	Register Clock (Phase 1)	F2	J2	J9	F9
C2	Register Clock (Phase 2)	F1	J1	J10	F10
C3	Register Clock (Phase 3)	G2	H2	H9	G9
SG	Summing Gate	E1	K1	K10	E10
RG	Reset Gate	E2	K2	K9	E9
OUT	Output	B1	N1	N10	B10

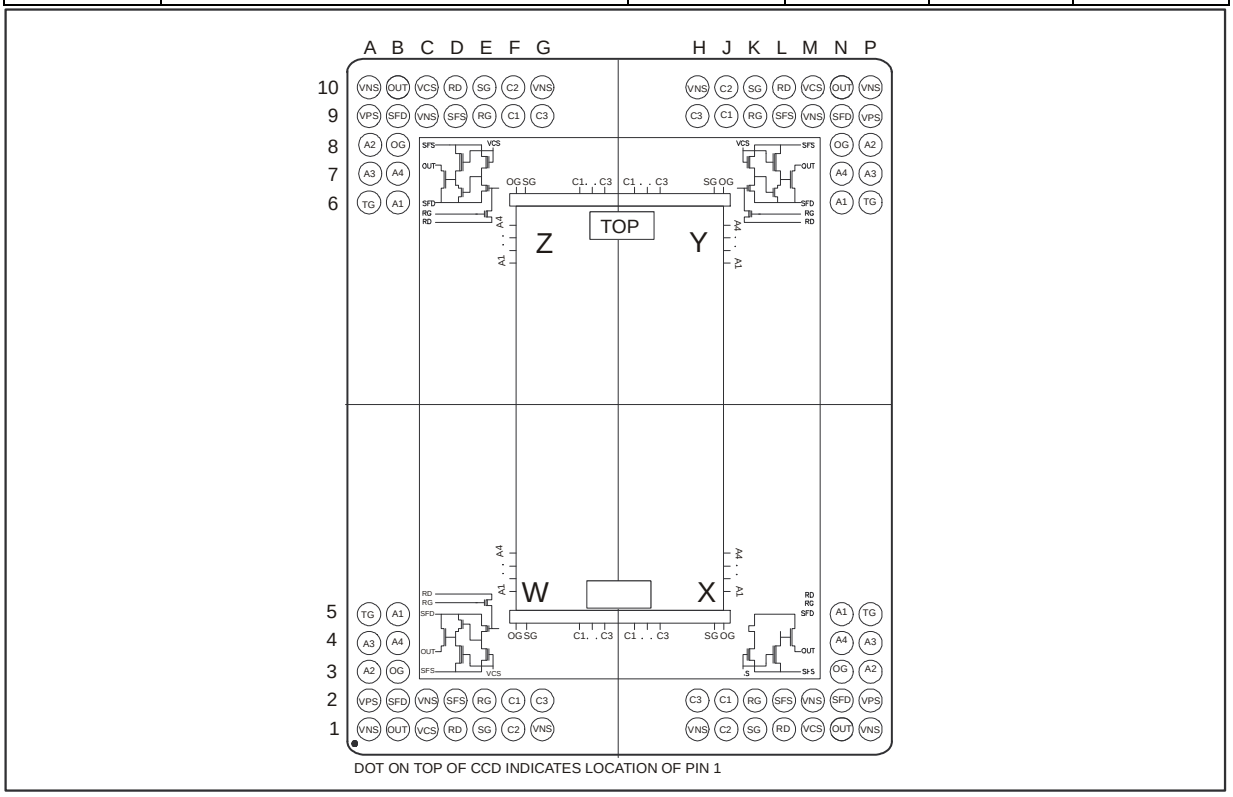
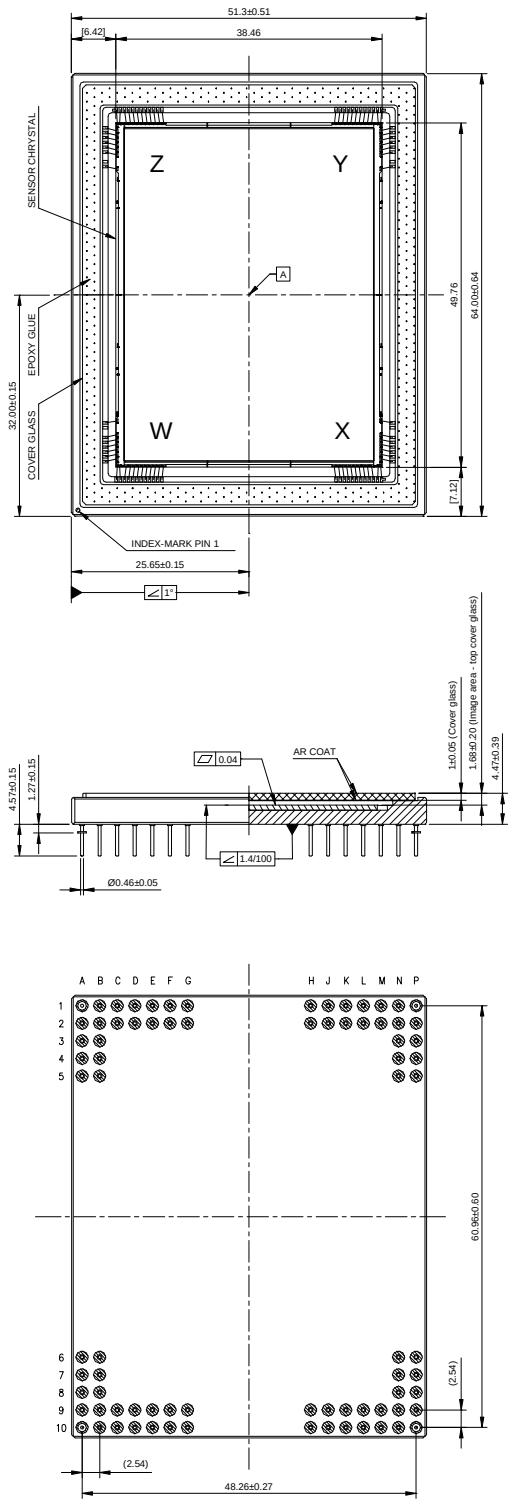


Figure 13 - Pin configuration (top view)



A is the center of the image area
Position of A:
25.65 ± 0.15 to left edge of package
32.00 ± 0.15 to lower edge of package
2.79 ± 0.15 to bottom of package

Angle of rotation: less then ± 1°
Sensor flatness: < 40 µm (P-V)

Cover glass: Hoya CG1
Thickness of cover glass: 1 ± 0.05
Refractive index: nd = 1.506
Double sided AR coating < 1% (430-660nm) reflection
Hermetically sealed package

All drawing units are in mm

Figure 14 – Mechanical drawing of the PGA package